Notice of Allowability	Application No.	Applicant(s)	
	10/812,301	MUELLER, PETER D.	
	Examiner	Art Unit	
	GREG BENGZON	2444	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Request for Continued Examination (RCE) filed 10/19/2009*.

2. ☒ The allowed claim(s) is/are *Claims 1-19, 21-30 renumbered Claims 1-29 respectively* .

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *1/12/2010* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/William C. Vaughn, Jr./
Supervisory Patent Examiner, Art Unit 2444

DETAILED ACTION

This application has been examined. Claims 1-19,21-30 are pending. Claim 20 is cancelled.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/19/2009 has been entered.

Priority

The effective date of the claims described in this application is March 29, 2004.

Information Disclosure Statement

The Applicant is respectfully reminded that each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in 37 CFR 1.56.

There were no information disclosure statements filed with this application.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Andy Kim,Reg.No. 61050 on January 12, 2010.

The application has been amended as follows:

IN THE CLAIMS:

1. (Currently amended) A management port for a wireless device platform, comprising:

a communication link *having a physical link*, local to a microprocessor subsystem, to be used in inter-processor communication over an inter-processor bus for the wireless device platform, the communication link to provide an inbound link and an outbound link,

the inbound link providing a path for communications from the inter- processor bus to a peripheral bus of the microprocessor subsystem, the inbound link receiving communications from at least one processor or peripheral communicating over the inter-processor bus,

the outbound link providing a path for communications from the peripheral bus of the microprocessor subsystem to the inter-processor bus, the outbound link transmitting communications over the inter-processor bus to the at least one processor or peripheral, and

the communication link to control data flow over the inbound and outbound links, the microprocessor subsystem comprising a processor core, at least one processor subsystem, and a microprocessor bus system, the microprocessor bus system providing a communication path between the processor core and the at least one processor subsystem; and

a management block to receive command data from the at least one processor or peripheral through a predetermined logic channel in the inbound link, the management block providing a corresponding command signal on the microprocessor bus system, *which relays the command signal to at least one processor or peripheral of the microprocessor subsystem,* the command signal performing a management function for the microprocessor *subsystem*, the management block being further adapted to receive a response signal from the microprocessor bus system and the management block transmitting corresponding response data through a predetermined logic channel in the outbound link to the at least one processor or peripheral via the inter-processor bus, the management block including a manageability control module,

the manageability control module configured to apply a protocol for communicating over the microprocessor bus system, and

the manageability control module configured to provide access for *allowing*

another microprocessor subsystem to perform the management function even when the processor core is not responsive to any signal .

2. (Previously Presented) The management port of claim 1, wherein the communication link includes a physical layer to provide both the inbound and outbound links with multiple logic channels, and a data link protocol to control data flow over the inbound and output links, and the management block provides the corresponding command signal directly on the microprocessor bus.

3. (Original) The management port of claim 1, wherein the management function includes a debug function.

4. (Original) The management port of claim 1, wherein the management function includes accessing memory.

5. (Original) The management port of claim 1, wherein the management function includes accessing configuration registers.

6. (Original) The management port of claim 1, wherein the management function includes accessing a peripheral device of the microprocessor system.

7. (Previously Presented) The management port of claim 1, wherein the

management block includes:

a command register connected to the microprocessor bus system and to the communication link, the command register to temporarily store the command data delivered through the predetermined logic channel in the inbound link;

a response register connected to the microprocessor bus system and to the communication link, the response register to temporarily store response data from the bus; and

a manageability controller connected to the microprocessor bus system, the command register, and the response register, the manageability controller being adapted to determine when command data is received at the command register and to transmit the corresponding command signal over the microprocessor bus system, and further being adapted to receive the response signal from the microprocessor bus system and store corresponding response data at the response register, and to transmit the response data through the predetermined logic channel in the outbound link.

8. (Currently Amended) A microprocessor system, comprising:

a processor core;

at least one processor subsystem to communicate with the processor core using at least one microprocessor bus;

a communication link connected to at least an inter-processor bus to enable inter- processor communication, the communication link to provide a multi-channel inbound link and a multi-channel outbound link, and to control data flow over a plurality

of channels for both the multi-channel inbound and outbound links,

the multi-channel inbound link providing a path for communications from the inter-processor bus to a peripheral bus of the microprocessor system, the multi-channel inbound link receiving communications from at least one processor or peripheral communicating over the inter-processor bus, and

the multi-channel outbound link providing a path for communications from the peripheral bus of the microprocessor system to the inter-processor bus, the multi-channel outbound link transmitting communications over the inter-processor bus to the at least one processor or peripheral; and

a management block to receive command data from the at least one processor or peripheral using a predetermined logic channel in the multi-channel inbound link, the management block providing a corresponding command signal on the at least one microprocessor bus, which relays the command signal to at least one processor or peripheral of the microprocessor system, the command signal performing a management function for at least one of the processor core and the at least one processor subsystem, the management block being further adapted to receive a response signal from the microprocessor bus and the management block transmitting corresponding response data through a predetermined logic channel in the outbound link to the at least one processor or peripheral via the inter-processor bus, the management block including a manageability control module,

the manageability control module configured to apply a protocol for communicating over the microprocessor bus, and

the manageability control module configured to provide access for allowing another microprocessor system to perform the management function even when the processor core is not ~~responsive,~~ responsive to any signal.

9. (Original) The microprocessor system of claim 8, wherein the management function includes a debug function.

10. (Original) The microprocessor system of claim 8, wherein the at least one processor subsystem includes a memory controller.

11. (Original) The microprocessor system of claim 8, wherein the at least one processor subsystem includes configuration registers.

12. (Original) The microprocessor system of claim 8, wherein the at least one processor subsystem includes a security module.

13. (Original) The microprocessor system of claim 8, wherein the at least one processor subsystem includes a Universal Serial Bus (USB) client.

14. (Previously Presented) The microprocessor system of claim 8, further comprising a peripheral device, the management block being adapted to generate the corresponding command signal on the at least one microprocessor bus to perform a management function for the at least one peripheral device.

15. (Currently Amended) A microprocessor system for a wireless device, comprising:

a processor core and at least one processor subsystem;

at least one bus to connect the processor core to the at least one processor subsystem;

means for providing a multi-channel inbound link and a multi-channel outbound link, connected to at least an inter-processor bus for inter-processor communication in the wireless device, and to control data flow over a plurality of channels for both the multi-channel inbound and outbound links;

the multi-channel inbound link providing a path for communications from the inter-processor bus to a peripheral bus of the microprocessor system, the multi-channel inbound link receiving communications from at least one processor or peripheral communicating over the inter-processor bus, and

the multi-channel outbound link providing a path for communications from the peripheral bus of the microprocessor system to the inter-processor bus, the multi-channel outbound link transmitting communications over the inter-processor bus to the at least one processor or peripheral; and

means for receiving command data from the at least one processor or peripheral through a predetermined logic channel in the inbound link, the means for receiving command data providing a corresponding command signal on the bus with an appropriate communication protocol to perform a management function for at least one processor ~~subsystem;~~ subsystem, the bus relaying the command signal to at least one processor or peripheral of the microprocessor system;

means for providing access for allowing another microprocessor system to perform the management function even when the processor core is not ~~responsive;~~

responsive to any signal; and

means for receiving a response signal from the bus and transmitting corresponding response data through a predetermined logic channel in the outbound link to the at least one processor or peripheral via the inter-processor bus.

16. (Previously Presented) The microprocessor system of claim 15, wherein the means for receiving command data and the means for receiving a response signal include a management block comprising:

a command register connected to the bus, the command register to temporarily store the command data delivered through the predetermined logic channel in the multi-channel inbound link;

a response register connected to the bus, the response register to temporarily store response data from the bus; and

a manageability controller connected to the bus, the command register, and the response register, the manageability controller being adapted to determine when the command data is received at the command register and to transmit the corresponding command signal over the bus, and further being adapted to receive the response signal from the bus and store the corresponding response data at the response register, and to transmit the response data through the predetermined logic channel in the multi-channel outbound link.

17. (Original) The microprocessor system of claim 15, wherein the means for

providing a multi-channel inbound link and a multi-channel outbound link for inter-processor communication in the wireless device includes means to provide a plurality of channels to communicate with an embedded communications microprocessor system.

18. (Original) The microprocessor system of claim 17, wherein the embedded communications microprocessor system is adapted to wirelessly communicate with at least one other devices.

19. (Currently Amended) A system, comprising:

an embedded applications microprocessor system and an embedded communications microprocessor system, each microprocessor system including a communication link to enable inter-processor communication over multiple channels;

a substantially omni-directional antenna connected to the embedded communications microprocessor system;

an inter-processor communication bus connected to the communication links of both the applications microprocessor system and the communications microprocessor system; and

the communication link of the applications microprocessor system being connected to at least an inter-processor bus, and including:

a multi-channel inbound link and a multi-channel outbound link, the communications link being adapted to control data flow over the multi-channel inbound and outbound links,

the multi-channel inbound link providing a path for communications from the inter-processor bus to a peripheral bus of the microprocessor system, the multi-channel

inbound link receiving communications from at least one processor or peripheral communicating over the inter-processor bus, and

the multi-channel outbound link providing a path for communications from the peripheral bus of the microprocessor system to the inter-processor bus, the multi-channel outbound link transmitting communications over the inter-processor bus to the at least one processor or peripheral; and

a manageability port to allow the communications microprocessor system to access a microprocessor bus local to the applications microprocessor system using at least one predetermined channel and to perform management functions in the applications microprocessor system, the manageability port:

being adapted to receive command data from the at least one processor or peripheral through a predetermined logic channel in the inbound link,

applying a protocol for communicating over the microprocessor bus, providing a corresponding command signal on the microprocessor bus, which relays the command signal to at least one processor or peripheral of the applications microprocessor system, and further is adapted to receive a response signal from the microprocessor bus,

providing access for allowing the communications microprocessor system to perform management functions even when a processor core of the applications microprocessor system is not ~~responsive,,~~ responsive to any signal, and

transmitting corresponding response data through a predetermined logic channel in the outbound link to the at least one processor or peripheral communicating over the inter- processor bus.

20. (Canceled)

21. (Previously Presented) The system of claim 19, wherein the embedded communications microprocessor system includes a microprocessor system adapted to wirelessly communicate with at least one other device.

22. (Original) The system of claim 21, wherein the microprocessor system is adapted to wirelessly communicate with at least one other devices using IEEE 802.11 technology.

23. (Original) The system of claim 21, wherein the microprocessor system is adapted to wirelessly communicate with at least one other device using cellular radio technology.

24. (Original) The system of claim 23, wherein the microprocessor is adapted to wirelessly communicate using general packet radio service (GPRS) technology.

25. (Original) The system of claim 23, wherein the microprocessor is adapted to wirelessly communicate using code division multiple access (CDMA) technology.

26. (Original) The system of claim 23, wherein the microprocessor is adapted to wirelessly communicate using wideband code division multiple access (WCDMA) technology.

27. (Original) The system of claim 19, the embedded communications

microprocessor system includes:

a microprocessor system adapted to wirelessly communicate with at least one other devices using an IEEE 802.11 technology; and

a microprocessor system adapted to wirelessly communicate with at least one other device using cellular radio technology.

28. (Currently Amended) A method, comprising:

receiving an inter-processor communication signal at a communications link for a microprocessor system, the communication link connected at least to an inter-processor bus, and used to provide a multi-channel inbound link and a multi-channel outbound link for the microprocessor system, and to control inter-processor data flow over the multi-channel inbound and outbound links, wherein receiving an inter-processor communication signal includes receiving a signal using a predetermined channel of the multi-channel inbound link, the signal including command data to perform a management function for a microprocessor subsystem,

the multi-channel inbound link providing a path for communications from the inter-processor bus to a peripheral bus of the microprocessor system, the multi-channel inbound link receiving communications from at least one processor or peripheral communicating over the inter-processor bus,

the multi-channel outbound link providing a path for communications from the peripheral bus of the microprocessor system to the inter-processor bus, the multi-channel outbound link transmitting communications over the inter-processor bus to the

at least one processor or peripheral;

processing the command data by a management block to generate and transmit a corresponding command signal on a microprocessor bus, which relays the command signal to at least one processor or peripheral of the microprocessor subsystem, the microprocessor bus local to the microprocessor system using an appropriate bus communication protocol to perform the management function; and

providing access by a management control block of the management block for allowing another microprocessor system to perform the management function even when a processor core of the microprocessor system is not ~~responsive,~~ responsive to any signal.

29. (Previously Presented) The method of claim 28, further comprising:

processing a response signal received over the microprocessor bus from the microprocessor subsystem into a response data; and

transmitting a signal that includes the response data using a predetermined channel of the outbound link.

30. (Original) The method of claim 29, wherein:

processing the command data includes routing the command data through a command register in preparation to transmit the corresponding command signal on the microprocessor bus; and

processing a response signal received over the microprocessor bus from the

microprocessor subsystem into response data includes routing the response data through a response register in preparation to transmit the signal that includes the response data using the predetermined channel on the outbound link.

Allowable Subject Matter

Claims 1-19,21-30 are allowed.

The following is an examiner's statement of reasons for allowance:

The provision for --- a management port for a wireless device platform, comprising:

a communication link having a physical ink, local to a microprocessor subsystem, to be used in inter-processor communication over an inter-processor bus for the wireless device platform, the communication link to provide an inbound link and an outbound link,

the inbound link providing a path for communications from the inter- processor bus to a peripheral bus of the microprocessor subsystem, the inbound link receiving communications from at least one processor or peripheral communicating over the inter-processor bus,

the outbound link providing a path for communications from the peripheral bus of the microprocessor subsystem to the inter-processor bus, the outbound link transmitting communications over the inter-processor bus to the at least one processor or peripheral, and

the communication link to control data flow over the inbound and outbound links,

the microprocessor subsystem comprising a processor core, at least one processor subsystem, and a microprocessor bus system, the microprocessor bus system providing a communication path between the processor core and the at least one processor subsystem; and

a management block to receive command data from the at least one processor or peripheral through a predetermined logic channel in the inbound link, the management block providing a corresponding command signal on the microprocessor bus system, *which relays the command signal to at least one processor or peripheral of the microprocessor subsystem,* the command signal performing a management function for the microprocessor subsystem, the management block being further adapted to receive a response signal from the microprocessor bus system and the management block transmitting corresponding response data through a predetermined logic channel in the outbound link to the at least one processor or peripheral via the inter-processor bus, the management block including a manageability control module,

the manageability control module configured to apply a protocol for communicating over the microprocessor bus system, and

the manageability control module configured to provide access for *allowing another microprocessor subsystem to perform the management function even when the processor core is not responsive to any signal*

--- wherein all the features previously described are combined in one singular embodiment, is not fairly taught or suggested by the prior art of record.

The Examiner finds particular novelty in the management port capabilities as described in the Applicant Specification (Page 6, Lines 1-10,Figure 4) wherein the management port is comprised of physical communication links and a management control module. The communication link provides a path for communications to and from the peripheral bus of the microprocessor subsystem to the inter-processor bus. The Examiner also find novelty in the management control module (page 10 Lines 15-25) wherein the said management control module is able receive a management function from a remote or external device via the communication link and relay *the command signal to at least one processor or peripheral of the microprocessor subsystem* such that the manageability control module configured to provide access for *allowing another microprocessor subsystem to perform the management function even when the processor core is not responsive to any signal.*

Narasimhan disclosed wherein network interface chip can act as a slave peripheral with a command based API (Application Programming Interface). As a peripheral, the network interface chip's API gives the equipment access to a monitoring and control protocol. In Monitoring and Control mode, the network interface chip uses a very simple protocol for allowing a remote client to access and control variables in the host system, and to make remote function calls. The internal data bus (see FIG. 12) of the network interface chip 36 connects directly to the device data bus. The NIC provides web-based or network-based management of any device. It also enables monitoring

and controlling of any device, regardless of its available processing power, code space, or interface pins. Even devices without a CPU or microcontroller are supported. The network interface chip will also support an external DMA (Direct Memory Access) if one is present in the device.

However Narasimhan does not disclose wherein the NIC provides a path for communications to and from the peripheral bus of the microprocessor subsystem to the inter-processor bus.

Furthermore Narasimhan does not disclose a management control module that is able receive a management function from a remote or external device via the communication link and relay *the command signal to at least one processor or peripheral of the microprocessor subsystem* such that the manageability control module configured to provide access for *allowing another microprocessor subsystem to perform the management function even when the processor core is not responsive to any signal*.

Bishop disclosed a logical inter-processor communication structure implemented by queue structure 145. Each simplex (one-way) virtual, or logical, communication channel 200 is a logical path, physically provided by bus 150, between two user processes 140 located on different processors 101.

However Bishop does not disclose a management control module that is able receive a management function from a remote or external device via the communication link and relay *the command signal to at least one processor or peripheral of the microprocessor subsystem* such that the manageability control module configured to

provide access for *allowing another microprocessor subsystem to perform the management function even when the processor core is not responsive to any signal*.

Kahle disclosed graceful recovery from a hang condition in a microprocessor. A hang condition refers to a processor state in which no new instructions are being completed by the processor. Hang conditions may originate from any of a variety of source including, as an example, a live lock condition in which the microprocessor is stuck in an endless state loop. The recovery sequence includes entering a relaxed execution mode, such as a debug mode, a serial operation mode, or an in-order mode prior to resuming processor operation.

However Kahle does not disclose a path for communications to and from the peripheral bus of the microprocessor subsystem to an inter-processor bus.

Furthermore Kahle does not disclose wherein a management control module is able *receive a management function from a remote or external device via the communication link* and relay *the command signal to at least one processor or peripheral of the microprocessor subsystem* such that the manageability control module configured to provide access for *allowing another microprocessor subsystem to perform the management function even when the processor core is not responsive to any signal*.

Osborne disclosed a network interface for a connection-based communication network that has support for remote operations with reply, such as a remote read operation, that bypass host computer interaction. The network interface 26 copies appropriate size chunks of the data from the host memory to the network interface and

forms the chunks of data into a packet for transmission into the network. In state of the art systems, such copying is typically performed by direct memory access (DMA).

However Osborne does not disclose a path for communications to and from the peripheral bus of the microprocessor subsystem to an inter-processor bus.

Furthermore Osborne does not disclose wherein a management control module is able *receive a management function from a remote or external device via the communication link* and relay *the command signal to at least one processor or peripheral of the microprocessor subsystem* such that the manageability control module configured to provide access for *allowing another microprocessor subsystem to perform the management function even when the processor core is not responsive to any signal*.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GREG BENGZON whose telephone number is (571)272-3944. The examiner can normally be reached on Mon. thru Fri. 8 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Vaughn can be reached on (571)272-3922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/G. B./
Examiner, Art Unit 2444

/William C. Vaughn, Jr./
Supervisory Patent Examiner, Art Unit 2444